WHAT IS CLAIMED IS:

1. A method for forming an oxide layer in an integrated circuit device process, comprising:

growing a thermal oxide layer on a surface of a semiconductor substrate in a chemical vapor deposition (CVD) apparatus; and

forming a CVD material layer on the thermal oxide layer in the CVD apparatus.

2. The method of claim 1, wherein the thermal oxide layer is formed to a thickness of approximately 20Å to 100Å.

3. The method of claim 1, wherein the CVD material layer is formed of a material selected from the group consisting of silicon oxide, aluminum oxide, zirconium oxide, and tantalum oxide.

4. The method of claim 1, further comprising: forming another material layer on the CVD material layer in the CVD apparatus.

5. The method of claim 1, wherein growing a thermal oxide layer comprises using O_2, N_2O or a combination thereof for an oxidizing ambient.

6. The method of claim 1, wherein growing a thermal oxide layer is carried out at a temperature of approximately 750°C to 1000°C.

7. The method of claim 1, wherein growing a thermal oxide layer is carried out at a temperature of approximately 750°C to 1000°C and forming a CVD material layer is carried out at a temperature of approximately 700°C to 850°C.

8. The method of claim 1, wherein the surface of the semiconductor substrate comprises a bottom and a sidewall of a trench formed by etching the substrate to a predetermined depth; and

wherein the thermal oxide layer is formed to a thickness of approximately 20Å to 100Å, and the CVD material layer is formed to a thickness of approximately 50Å to 400Å.

9. The method of claim 8, wherein the CVD material layer is formed of a material selected from the group consisting of silicon oxide, aluminum oxide, zirconium oxide, and tantalum oxide.

10. The method of claim 8, wherein growing a thermal oxide layer uses O_2, N_2O or a combination thereof as a source gas at a temperature of approximately 750°C to 1000°C, and forming a CVD material layer is carried out using N_2O and SiH_4 as source gases at a temperature of approximately 700°C to 850°C.

11. The method of claim 8, further comprising: forming a nitride liner layer on the CVD material layer in the CVD apparatus to a thickness of approximately 30Å to 100Å, and forming a trench filling layer on the nitride liner layer in the CVD apparatus to a thickness of approximately 3000Å to 10000Å.

12. A method of forming an oxide layer in an integrated circuit device process, comprising:

forming a thermal oxide layer on an exposed single crystalline silicon substrate in a chemical vapor deposition (CVD) apparatus; and

forming a CVD material layer on the thermal oxide layer in the CVD apparatus.

13. The method of claim 12, wherein forming a thermal oxide layer is carried out at a temperature of approximately 750°C to 1000°C, and forming a CVD material layer is carried out at a temperature of approximately 700°C to 850°C.

14. The method of claim 13, wherein O_2, N_2O or combination thereof is used as a source gas for forming a thermal oxide layer, and N_2O and SiH_4 are used as a source gas for forming a CVD material layer.

15. A method of forming a layer for an integrated circuit device, comprising:

forming a trench in a single crystalline silicon substrate by etching;

forming a thermal oxide layer on a surface of the trench;

forming a conformal liner material layer on the thermal oxide layer; and

forming a nitride liner layer on the conformal liner material layer.

16. The method of claim 15, wherein the thermal oxide layer is formed to a thickness of 20Å to 100Å.

17. The method of claim 15, wherein the liner material layer is formed to a thickness of 50Å to 400Å.

18. The method of claim 15, wherein the liner material layer is made of a material selected from the group consisting of silicon dioxide, aluminum trioxide, zirconium oxide, and tantalum pentoxide.

19. The method of claim 15, wherein the thermal oxide layer, the liner material layer, and the nitride liner layer are formed in the same chemical vapor deposition (CVD) apparatus.

20. The method of claim 19, wherein the thermal oxide layer is formed using O_2, N_2O or a combination thereof as a source gas at a temperature of approximately 750°C to 1000°C, and the liner material layer is a high temperature oxide layer formed using N_2O and SiH_4 as a source gas at a temperature of approximately 700°C to 850°C.

21. The method of claim 20, further comprising: forming a trench isolation material on the nitride liner layer in the same CVD apparatus to fill the trench.

22. A method of forming an isolation trench, comprising,

etching a single crystalline silicon substrate to form a trench therein; and

forming all layers, formed in the trench, in the trench in the same chemical vapor deposition (CVD) apparatus.

23. The method of claim 22, wherein said all layers include a thermal oxide layer formed directly following formation of the trench, a liner material barrier layer formed on the thermal oxide layer, a nitride liner layer formed on the liner material barrier layer, and a trench isolation material layer formed on the nitride liner layer to fill the trench.

24. The method of claim 23, wherein the thermal oxide layer is formed to a thickness of 20Å to 100Å, and the liner material barrier layer is formed to a thickness of 50Å to 400Å.

25. The method of claim 23, wherein the thermal oxide layer is formed using O_2, N_2O or a combination thereof as a source gas at a temperature of approximately 750°C to 1000°C, and the liner material layer is a higher temperature oxide layer formed using N_2O and SiH_4 as a source gas at a temperature of approximately 700°C to 850°C.

26. The method of claim 23, wherein the liner material layer is made of a material selected from the group consisting of silicon oxide, aluminum oxide, zirconium oxide, and tantalum oxide.

27. A trench isolation structure comprising:

a trench for device isolation formed in a semiconductor substrate to a predetermined depth;

a thermal oxide layer formed on a bottom and a sidewall of the trench to a thickness of 20Å to 100Å;

a chemical vapor deposition (CVD) material barrier layer formed on the thermal oxide layer to a thickness of 50Å to 400Å;

a nitride liner layer formed on the CVD material barrier layer; and

a trench isolation material layer formed on the nitride liner layer to fill up the trench.

28. The trench isolation structure of claim 27, wherein thermal oxide layer and the CVD material barrier layer are formed in the same CVD apparatus, and the CVD material barrier layer is made of aluminum oxide.